ABSTRACT OF THE DISCLOSURE

The present invention provides a parallel arithmetic apparatus capable of easily performing vector inner product operations as well as efficient matrix operations. The parallel arithmetic apparatus is provided with pairs of registers that record arithmetical elements to be operated and FMACs that perform sum-of-products operations based on the arithmetical elements recorded in these registers, and selectors inserted between the register and FMAC. The selectors input the arithmetical element recorded in the register to the FMAC during a matrix operation, select the registers one by one in a round-robin fashion and supply the arithmetical element recorded in the selected register to the FMAC during a vector inner product operation.